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EXAMINER	
PHAM, HOAI V	

ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/085,164	KELLY ET AL.	
	Examiner	Art Unit	
	Hoai v. Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/25/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18,20-35,37-43 and 51-65* is/are pending in the application.

4a) Of the above claim(s) *51-65* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18,20-35 and 37-43* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/29/2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The finality of the previous Office action dated 7/25/2006 is hereby withdrawn.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 10 and 39 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The limitation "further comprising length and width dimensions of approximately .079 milimeters and .065 milimeters (.050 milimeters), respectively, and a height dimension of approximately .032 milimeters" are not supported in the specification and the drawing.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-8, 12, 13, 15-18 and 42-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakayama et al. [U.S. Pat. 6,208,023] previously applied.

With respect to claim 1, Nakayama et al. (figs. 1a-1c, cols. 9-13) discloses a packaged semiconductor device, comprising:

a semiconductor die (11);

a substrate (12), with the semiconductor die disposed therein;

a plurality of leads (15) coupled to the semiconductor die (11), wherein at least one of said lead has a shaped end proximate the substrate and inherently configured to minimize parasitic capacitance over a predetermined frequency range since the end of the leads (15) is smaller than the substrate (12), thus the capacitance is smaller compared to the end of the leads that have the equal or greater size than the substrate;

an encapsulant (17) enclosing the semiconductor die (11) and plurality of leads(15), the encapsulant inherently having a consistant dielectric constant over a predetermined frequency range; and

the encapsulant inherently operable to shunt thermal capacitance and thermal resistance away from the semiconductor die (11). It is noted that, resin material are used as insulating materials such as adhesives, insulating films and sealing materials, wherein resin materials are excellent in heat resistance, dielectric properties, etc. Therefore, the encapsulant (17, resin) is inherently having a consistent dielectric

constant over a predetermined frequency range and operable to shunt thermal capacitance and thermal resistance away from the semiconductor die.

With respect to claim 2, Nakayama et al. discloses an I/O common terminal (12, 14) (col. 11, lines 4-11), at least one input terminal (15) and at least one output terminal (15), coupled to the semiconductor die (11) (fig. 1a, col. 9, lines 59-65).

With respect to claim 3, Nakayama et al. discloses that wherein the input terminal (15) and output terminal (15) are positioned orthogonal to the I/0 common terminal (12, 14) (fig. 1c).

With respect to claim 4, Nakayama et al. discloses that the semiconductor die (11) is positioned above the I/0 common terminal (12, 14) (fig. 1c).

With respect to claim 5, Nakayama et al. discloses that the encapsulant (17) forms a substantially hexagonal structure surrounding the I/0 common terminal (12, 14), input terminal (15), and output terminal (15), essentially at right angles with respect to the substrate (fig. 1b).

With respect to claim 6, it is inherent a lead-frame for coupling the input terminal (15) to a circuit and the output terminal (15) to a circuit.

With respect to claim 7, Nakayama et al. discloses that the portion of the lead-frame coupled to each of the input terminal (15) and output terminal (15) possess exposed dovetailed side edges operable to allow epoxy to lock on the sides and top of the exposed edges (fig. 1b).

With respect to claim 8, Nakayama et al. discloses that the an end surface of the input terminal (15) being positioned adjacent and parallel to the side surface of the I/0

common terminal (12, 14), and an end surface of the output terminal (15) being positioned adjacent and parallel to the opposing side surface of the I/0 common terminal, said end surfaces being shaped so as to minimize parasitic capacitance (figs. 1a-1c).

With respect to claims 12 and 43, Nakayama et al. discloses that the packaged semiconductor device used in a surface mount assembly (col. 10, lines 51-63).

With respect to claim 13, Nakayama et al. discloses that the packaged semiconductor device used in an integrated circuit (col. 9, lines 56-58).

With respect to claim 15, Nakayama et al. discloses that the metallization, including a first and second metallization strip (16A), as the means of coupling the input terminal (15) and the output terminal (15) to the semiconductor die (11) (fig. 1b).

With respect to claim 16, Nakayama et al. discloses that a path length from input terminal (15) to the output terminal (15), of a fraction of the wavelength for which frequency the semiconductor device is designed (fig. 1b, col. 11, lines 12-15).

With respect to claim 17, Nakayama et al. discloses that bond wires (16A) as the means of coupling the input terminal (15) and the output terminal (15) to the semiconductor die, the input terminal being coupled to a first end of a first bond wire (16A), a second end of the first bond wire being coupled to the semiconductor die (11), a first end of a second bond wire (16A) being coupled to the semiconductor die (11), a second end of the second bond wire being coupled to the output terminal (15) (fig. 1b).

With respect to claim 18, Nakayama et al. discloses that a path length from the input terminal to the output terminal of a fraction of the wavelength for which frequency the semiconductor device is designed (fig. 1b, col. 11, lines 12-15).

With respect to claim 42, Nakayama et al. (figs. 1a-1c, cols. 9-13) discloses a packaged semiconductor device, comprising:

a semiconductor die (11), a substrate (12), and a plurality of leads (15), wherein at least one of said lead has a shaped end inherently configured to minimize parasitic capacitance over a predetermined frequency range since the end of the leads (15) is smaller than the substrate (12), thus the capacitance is smaller compared to the end of the leads that have the equal or greater size than the substrate;

a semiconductor die (11) being disposed in the substrate (12);

a coupling means from the plurality of leads (15) to the semiconductor die (11) for providing low capacitance electrical connections which supports device functionality; and

an encapsulation material surrounding the semiconductor die, plurality of leads and coupling means, the encapsulation material making contact with the substrate operable to allow direct dissipation shunting to thermal ground, the encapsulation material having a consistent dielectric constant over the predetermined frequency range. It is noted that, resin material are used as insulating materials such as adhesives, insulating films and sealing materials, wherein resin materials are excellent in heat resistance, dielectric properties, etc. Therefore, the encapsulant (17, resin) is

inherently having a consistent dielectric constant over a predetermined frequency range and operable to allow direct dissipation shunting to thermal ground.

5. Claims 1-4, 8-9, 12-13, 15, 17 and 42-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Crowley et al. [U.S. Pat. 6,753,597] previously applied.

With respect to claim 1, Crowley et al. (fig. 7, col. 6) discloses a packaged semiconductor device, comprising:

a semiconductor die (32);

a substrate (72), with the semiconductor die disposed therein;

a plurality of leads (38) coupled to the semiconductor die (32), wherein at least one of said lead has a shaped end proximate the substrate and inherently configured to minimize parasitic capacitance over a predetermined frequency range since the end of the leads (38) is thinner than the lead (38) itself and smaller than the substrate (12), thus the capacitance is smaller compared to the end of the leads that have the equal or greater size than the substrate;

an encapsulant (77) enclosing the semiconductor die (32) and plurality of leads (38), the encapsulant inherently having a consistant dielectric constant over a predetermined frequency range; and

the encapsulant inherently operable to shunt thermal capacitance and thermal resistance away from the semiconductor die (32). It is noted that, resin material are used as insulating materials such as adhesives, insulating films and sealing materials, wherein resin materials are excellent in heat resistance, dielectric properties, etc.

Therefore, the encapsulant (77, epoxy resin) is inherently having a consistent dielectric constant over a predetermined frequency range and operable to shunt thermal capacitance and thermal resistance away from the semiconductor die.

With respect to claim 2, Crowley et al. discloses an I/O common terminal (72) at least one input terminal (38) and at least one output terminal (38), coupled to the semiconductor die (32) (fig. 7).

With respect to claim 3, Crowley et al. discloses that wherein the input terminal (38) and output terminal (38) are positioned orthogonal to the I/0 common terminal (72) (fig. 7).

With respect to claim 4, Crowley et al. discloses that the semiconductor die (32) is positioned above the I/0 common terminal (72) (fig. 7).

With respect to claim 8, Crowley et al. discloses that the an end surface of the input terminal (38) being positioned adjacent and parallel to the side surface of the I/0 common terminal (72), and an end surface of the output terminal (38) being positioned adjacent and parallel to the opposing side surface of the I/0 common terminal, said end surfaces being shaped so as to minimize parasitic capacitance (fig. 7).

With respect to claim 9, Crowley et al. discloses that the leadframe terminal (38) has a rounded shaped on the end surface (fig. 4).

With respect to claims 12 and 43, Crowley et al. discloses that the packaged semiconductor device used in a surface mount assembly (fig. 7).

With respect to claim 13, Crowley et al. discloses that the packaged semiconductor device used in an integrated circuit (col. 1, lines 23-24).

With respect to claim 15, Crowley et al. discloses that the metallization, including a first and second metallization strip (46), as the means of coupling the input terminal (38) and the output terminal (38) to the semiconductor die (32) (fig. 7).

With respect to claim 17, Crowley et al. discloses that bond wires (46) as the means of coupling the input terminal (38) and the output terminal (38) to the semiconductor die, the input terminal being coupled to a first end of a first bond wire (46), a second end of the first bond wire being coupled to the semiconductor die (32), a first end of a second bond wire (38) being coupled to the semiconductor die (32), a second end of the second bond wire being coupled to the output terminal (38) (fig. 7).

With respect to claim 42, Crowley et al. (fig. 7, col. 6) discloses a packaged semiconductor device, comprising:

a semiconductor die (32), a substrate (72), and a plurality of leads (38), wherein at least one of said lead has a shaped end inherently configured to minimize parasitic capacitance over a predetermined frequency range since the end of the leads (38) is smaller than the substrate (72), thus the capacitance is smaller compared to the end of the leads that have the equal or greater size than the substrate;

a semiconductor die (32) being disposed in the substrate (72);

a coupling means from the plurality of leads (38) to the semiconductor die (32) for providing low capacitance electrical connections which supports device functionality; and

an encapsulation material (77) surrounding the semiconductor die, plurality of leads and coupling means, the encapsulation material making contact with the substrate

operable to allow direct dissipation shunting to thermal ground, the encapsulation material having a consistent dielectric constant over the predetermined frequency range. It is noted that, resin material are used as insulating materials such as adhesives, insulating films and sealing materials, wherein resin materials are excellent in heat resistance, dielectric properties, etc. Therefore, the encapsulant (17, resin) is inherently having a consistent dielectric constant over a predetermined frequency range and operable to allow direct dissipation shunting to thermal ground.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. [U.S. Pat. 6,208,023] previously applied or Crowley et al. [U.S. Pat. 6,753,597] previously applied.

With respect to claim 11, Nakayama et al. or Crowley et al. substantially discloses all the limitations as claimed above except an operating frequency range from DC to 10 gigahertz. However, the operating frequency range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

With respect to claim 14, Nakayama et al. or Crowley et al. substantially discloses all the limitations as claimed above except the packaged semiconductor device used in an amplifier gain stages. However, it is obvious to the skilled in the art to use the packaged semiconductor device in an amplifier gain stages because it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from the prior art

apparatus satisfying the claimed structure limitations. *Ex parte Masham, 2USPQ2d 1647* (1987).

9. Claims 20-27, 29-32, 34-35, 37-38, and 40-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. [U.S. Pat. 6,208,023] previously applied, in view of Ishinaga [U.S. Pat. 5,936,264] previously applied.

With respect to claims 20-21, Nakayama et al. does not disclose a light emitting diode as the semiconductor die. However, Ishinaga discloses that it is known in the art a light emitting diode can be used as the semiconductor die (chip) (see col.1, lines 22-27). Therefore, it would have been obvious to the skilled in the art to use the semiconductor die as the light emitting diode as taught by Ishinaga into the device of Nakayama et al. to use as the light emitting diode device.

With respect to claim 22, Nakayama et al. does not disclose a substantially clear epoxy material as the encapsulant. However, Ishinaga discloses that the encapsulant is clear epoxy material (see col. 3, lines 24-27). Therefore, it would have been obvious to the skilled in the art to use clear epoxy material for the encapsulant as taught by Ishinaga into the device of Nakayama et al. in order to allow the light emitted from the LED chip to be transmitted therethrough.

With respect to claims 23, 26 and 31, Nakayama et al. discloses a cathode (terminal 15) and an anode (terminal 15) as the plurality of leads.

With respect to claim 24, Nakayama et al. discloses that the positioning of the cathode (terminal 15) and the anode (terminal 15) opposite to each other (fig. 1c).

With respect to claim 25, Nakayama et al. discloses an encapsulant (17) with a substantially hexagonal structure around the cathode (terminal 15) and the anode (terminal 15) essentially at right angles with respect to the substrate (12) (fig. 1b).

With respect to claim 27, Nakayama et al. discloses that a shaped end surface of the cathode inherently operable to minimize parasitic capacitance.

With respect to claim 29, Nakayama et al. discloses metallization (16A) as the cathode coupling means to the semiconductor die (11) (fig. 1b).

With respect to claim 30, Nakayama et al. discloses a bond wire (16A) as the means of coupling the cathode to the semiconductor die (11), a first end of the bond wire being coupled to the cathode and a second end of the bond wire being coupled to the semiconductor die (11) (fig. 1c).

With respect to claim 32, Nakayama et al. discloses that a shaped end surface of the anode inherently operable to minimize parasitic capacitance.

With respect to claim 34, Nakayama et al. discloses metallization (16A) as the anode coupling means to the semiconductor die (11) (fig. 1b).

With respect to claim 35, Nakayama et al. discloses a bond wire (16A) as the means of coupling the anode to the semiconductor die (11), a first end of the bond wire being coupled to the anode and a second end of the bond wire being coupled to the semiconductor die (11) (fig. 1c).

With respect to claim 37, Nakayama et al. discloses that the packaged semiconductor device used in an integrated circuit (col. 9, lines 56-58).

With respect to claim 38, Nakayama et al. discloses that the packaged semiconductor device used in a surface mount assembly (col. 10, lines 51-63).

With respect to claim 40, Nakayama et al. (figs. 1a-1c, cols. 9-13) discloses a packaged semiconductor device, comprising:

a substrate (12), a terminal (15), and an encapsulant material (17);

a semiconductor die (11) being disposed in the substrate;

a means coupling the terminal (15) to the semiconductor die (11);

the terminal further comprising a terminal shaped end configured to minimize parasite capacitance over a predetermined frequency range;

a substantially encapsulant (17) for encapsulating the semiconductor die (11), the encapsulant material acting as a thermal shunt to ground operable to decrease thermal capacitance and thermal resistance.

Nakayama et al. does not disclose a light emitting diode as the semiconductor die and a substantially clear epoxy material as the encapsulant. However, Ishinaga discloses that it is known in the art a light emitting diode can be used as the semiconductor die (chip) (see col.1, lines 22-27) and the encapsulant is clear epoxy material (see col. 3, lines 24-27). Therefore, it would have been obvious to the skilled in the art to use the semiconductor die as the light emitting diode as taught by Ishinaga into the device of Nakayama et al. to use as the light emitting diode device. It would have been obvious to the skilled in the art to use clear epoxy material for the encapsulant as taught by Ishinaga into the device of Nakayama et al. in order to allow the light emitted from the LED chip to be transmitted therethrough.

With respect to claim 41, Nakayama et al. discloses that the packaged semiconductor device used in a surface mount assembly (col. 10, lines 51-63).

10. Claims 20-24, 26-35, 37-38, and 40-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crowley et al. [U.S. Pat. 6,753,597] previously applied, in view of Ishinaga [U.S. Pat. 5,936,264] previously applied.

With respect to claims 20-21, Crowley et al. does not disclose a light emitting diode as the semiconductor die. However, Ishinaga discloses that it is known in the art a light emitting diode can be used as the semiconductor die (chip) (see col.1, lines 22-27). Therefore, it would have been obvious to the skilled in the art to use the semiconductor die as the light emitting diode as taught by Ishinaga into the device of Crowley et al. to use as the light emitting diode device.

With respect to claim 22, Crowley et al. does not disclose a substantially clear epoxy material as the encapsulant. However, Ishinaga discloses that the encapsulant is clear epoxy material (see col. 3, lines 24-27). Therefore, it would have been obvious to the skilled in the art to use clear epoxy material for the encapsulant as taught by Ishinaga into the device of Crowley et al. in order to allow the light emitted from the LED chip to be transmitted therethrough.

With respect to claims 23, 26 and 31, Crowley et al. discloses a cathode (terminal 38) and an anode (terminal 38) as the plurality of leads (fig. 7).

With respect to claim 24, Crowley et al. discloses that the positioning of the cathode (terminal 38) and the anode (terminal 38) opposite to each other (fig. 7).

With respect to claim 27, Crowley et al. discloses that a shaped end surface of the cathode inherently operable to minimize parasitic capacitance (fig. 7).

With respect to claims 28 and 33, Crowley et al. discloses that the leadframe terminal (38) has a rounded shape on the end surface (fig. 4).

With respect to claim 29, Crowley et al. discloses metallization (46) as the cathode coupling means to the semiconductor die (32) (fig. 7).

With respect to claim 30, Crowley et al. discloses a bond wire (46) as the means of coupling the cathode to the semiconductor die (32), a first end of the bond wire being coupled to the cathode and a second end of the bond wire being coupled to the semiconductor die (32) (fig. 7).

With respect to claim 32, Crowley et al. discloses that a shaped end surface of the anode inherently operable to minimize parasitic capacitance (fig. 7).

With respect to claim 34, Crowley et al. discloses metallization (46) as the anode coupling means to the semiconductor die (32) (fig. 7).

With respect to claim 35, Crowley et al. discloses a bond wire (46) as the means of coupling the anode to the semiconductor die (32), a first end of the bond wire being coupled to the anode and a second end of the bond wire being coupled to the semiconductor die (32) (fig. 7).

With respect to claim 37, Crowley et al. discloses that the packaged semiconductor device used in an integrated circuit (col. 1, lines 23-24).

With respect to claim 38, Crowley et al. discloses that the packaged semiconductor device used in a surface mount assembly (fig. 7).

With respect to claim 40, Crowley et al. (fig. 7, col. 6) discloses a packaged semiconductor device, comprising:

a substrate (72), a terminal (38), and an encapsulant material (77);

a semiconductor die (32) being disposed in the substrate;

a means coupling the terminal (38) to the semiconductor die (32);

the terminal further comprising a terminal shaped end configured to minimize parasite capacitance over a predetermined frequency range;

a substantially encapsulant (77) for encapsulating the semiconductor die (32), the encapsulant material acting as a thermal shunt to ground operable to decrease thermal capacitance and thermal resistance.

Crowley et al. does not disclose a light emitting diode as the semiconductor die and a substantially clear epoxy material as the encapsulant. However, Ishinaga discloses that it is known in the art a light emitting diode can be used as the semiconductor die (chip) (see col.1, lines 22-27) and the encapsulant is clear epoxy material (see col. 3, lines 24-27). Therefore, it would have been obvious to the skilled in the art to use the semiconductor die as the light emitting diode as taught by Ishinaga into the device of Crowley et al. to use as the light emitting diode device. It would have been obvious to the skilled in the art to use clear epoxy material for the encapsulant as taught by Ishinaga into the device of Crowley et al. in order to allow the light emitted from the LED chip to be transmitted therethrough.

With respect to claim 41, Crowley et al. discloses that the packaged semiconductor device used in a surface mount assembly (fig. 7).

11. Claims 9, are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. [U.S. Pat. 6,208,023] previously applied, in view of Crowley et al. [U.S. Pat. 6,753,597] previously applied.

Nakayama et al. substantially discloses all the limitations as claimed above except the configured lead has a rounded shape expanding outward toward the substrate. However, Crowley et al. discloses the leadframe terminal (38) has a rounded shape on the end surface. Therefore, it would have been obvious to the skilled in the art to modify the input and output terminals with the rounded shape on the end surface as taught by Crowley et al. into the device of Nakayama et al. because the round shape would reduce the material, would improve in the locking strength to the encapsulation and would inherently reduce parasitic capacitance.

12. Claims 28 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. [U.S. Pat. 6,208,023] in view of Ishinaga [U.S. Pat. 5,936,264] as applied to claims 1, 20, 23, 27 and 32 above, and further in view of Crowley et al. [U.S. Pat. 6,753,597].

Nakayama et al. in view of Ishinaga substantially disclose all the limitations as claimed above except a rounded shape on the end surface of the cathode and anode. However, Crowley et al. (fig. 4) discloses the leadframe terminal (38) has a rounded shape on the end surface. Therefore, it would have been obvious to the skilled in the art to modify the input and output terminals with the rounded shape on the end surface as taught by Crowley et al. into the device of Nakayama et al. because the round shape

would reduce the material, would improve in the locking strength to the encapsulation and would inherently reduce parasitic capacitance.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai v. Pham whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HOAI PHAM
PRIMARY EXAMINER